- In claim 3, at line 4, **delete** "premelting" and **insert** – pre-melting -- after "conditioning and".
- In claim 5, at line 5, **delete** "joining" and **insert** -- bonding -- after "process of".
- In claim 21, at line 3, **delete** "side" after "surface".
- In claim 21, at line 5, **delete** "side" -- after "surface".
- In claim 21, at line 9, **insert** -- the -- after "layer of".
- In claim 21, at line 13, **insert** -- the -- after "layer of".
- **CANCEL** claims 11-19.

Change(s) applied to document, /J.C.J/ 11/28/2011

Allowable Subject Matter

5. Claims 1-9 and 21-22 are allowed. The following is an examiner's statement of reasons for allowance:

The prior art does not teach or suggest a process having all of the limitations of **claim 1**, including: providing patterned layers of the electrically non-conducting glass paste and the electrically conducting glass paste on said wafer surfaces, wherein the wafers are processed semiconductor wafers having electrically active structures thereon, and thereafter conditioning and pre-melting the electrically non-conducting glass paste and the electrically conducting glass paste, and thereafter bonding the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste and at a second processing temperature of the